







The DEEP-SEA Project

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DEEP-SEA SW Stack





Public release at https://gitlab.jsc.fz-juelich.de/deep-sea/wp3/software/easybuild-repository-deep-sea

DEEP-SEA: Optimisation Cycles

Bewildering variety of SW tools available to HPC SW developers for analysis and optimisation – in DEEP-SEA alone, these:



Optimisation cycles encapsulate (complex) tool workflows for specific purposes

- For instance, assessing load balance or optimising energy use

They guide SW developers and make it easier to achieve specific goals

- Rather then using specific tools

You'll hear much more about Optimisation Cycles in the 13:30 presentation

DEEP-SEA & Heterogeneous Memory

- Examples...
 - DDR DRAM
 - Scratchpad (Embedded systems-on-chip, GPUs)
 - High bandwidth memory (Intel Xeon Phi, GPUs)
 - Byte addressable non-volatile memory (HP's Machine, Intel Optane)
 - Compute Express Link (CXL): high-speed interface to accelerators and memory modules





DEEP-SEA & Memory Tools

- How much, if any, do the applications need to be modified?
- Which layer manages the memory? When?
- How much can the applications benefit?



2.5

3.0

3.5

DEEP-SEA & Malleability

- Usual HPC workload resource reservation (constant # cores or nodes over time)
- Actual use of resources varies over time (yellow curve)
- Workload is able to use more resources in certain phases (arrow)
- Ideal resource allocation for the workload
- Malleable applications
 - Release resources not required
 - Acquire more resources if advantageous
- Resource management systems & fabrics must support this
- Change in # of nodes do require data redistribution in the workload



time

nodes

es



DEEP-SEA & Scheduling

DEEP-SEA Co-Design Applications



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